Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (cancelled)

2. (cancelled)

3. (currently amended): The ball grid array package semiconductor device of claim [[1]] 16, wherein the device is a chip scale package semiconductor device.

4. (currently amended): The ball grid array package semiconductor device of claim [[1]] 16, wherein the first power has a positive voltage and the second power is ground.

5. (withdrawn): The ball grid array package semiconductor device of claim 4, wherein the semiconductor chip comprises a triple-well structure having a P-substrate, the first power is applied to an N-well of the semiconductor chip, and the second power is applied to the P-substrate and a pocket P-well of the semiconductor chip.

6. (withdrawn): The ball grid array package semiconductor device of claim 4, wherein the semiconductor chip comprises a triple-well structure having a P-substrate, the first power is applied to an N-well of the

semiconductor chip, and the second power is applied to one of the P-substrate and a pocket P-well of the semiconductor chip.

7. (withdrawn): The ball grid array package semiconductor device of claim 4, wherein the semiconductor chip comprises a twin-well structure, the first power is applied to an N-well of the semiconductor chip, and the second power is applied to a P-substrate of the semiconductor chip.

8. (withdrawn): A ball grid array package semiconductor device, the device being supplied with two or more external powers, the device comprising:

a semiconductor chip having a pad at its center of a surface thereof;

a substrate having a slot of a predetermined size and centrally arranged in a spaced relationship to the pad, the substrate having a signal line plane including a signal line pattern and a plurality of ball mounts on its one side, and wherein the semiconductor chip is mounted on an other side thereof;

a bonding material inserted between the semiconductor chip and the substrate to fix the semiconductor chip to the substrate; and

a plurality of balls mounted on the plurality of ball mounts to be connected to an external circuit,

wherein the signal line plane is divided into a plurality of signal line planes, and lines for at least one selected power among the external powers are formed only on a corresponding signal line plane.

9. (withdrawn): The ball grid array package semiconductor device of claim 8, wherein the lines for the at least one selected power among the external powers are combined with each other on the corresponding signal line plane, thereby forming a combined plane exhibiting a single node electrically.

10. (withdrawn): The ball grid array package semiconductor device of claim 8, wherein the device is a chip scale package semiconductor device.

11. (cancelled)

12. (cancelled)

13. (cancelled)

14. (cancelled)

15. (cancelled)

16. (new): A ball grid array package semiconductor device, the device being supplied with two or more external powers including a first power and a second power, the device comprising:

a semiconductor chip having a plurality of pads arranged along a first surface thereof;

a substrate having a first surface which confronts the first surface of the semiconductor chip and an opposite second surface, the substrate further having a slot extending there through which is aligned over the plurality of pads to expose the plurality of pads;

a bonding material inserted between the respective first surfaces of the semiconductor chip and the substrate to fix the semiconductor chip to the substrate;

a first power plane located over the second surface of the substrate on one side only of the slot, wherein the first power plane is electrically connected to at least one of the plurality of pads through the slot;

a second power plane located over the second surface of the substrate on another side only of the slot, wherein the second power plane is electrically connected to at least one of the plurality of pads through the slot;

a first plurality signal ball mounts located within the first power plane and electrically isolated from the first power plane;

a first plurality of signal lines extending from the respective first plurality of signal ball mounts to a peripheral region of the first power plane, wherein the first plurality of signal lines extend through respective gaps in the first power plane and are electrically isolated from the first power plane;

a first plurality of wirings extending through the slot and connected between the respective first plurality of signal lines and respective ones of the plurality of pads;

a second plurality of signal ball mounts located within the second power plane and electrically isolated from the second power plane;

a second plurality of signal lines extending from the respective second plurality of signal ball mounts to a peripheral region of the second power plane, wherein the second plurality of signal lines extend through respective gaps in the second power plane and are electrically isolated from the second power plane;

a second plurality of wirings extending through the slot and connected between the respective second plurality of signal lines and respective ones of the plurality of pads;

a first plurality power ball mounts located within the first power plane and electrically contacting the first power plane;

a second plurality of power ball mounts located within the second power plane and electrically contacting the second power plane;

a plurality of signal balls respectively mounted on the first and second pluralities of signal ball mounts and electrically isolated from the first and second power planes;

a first plurality of power balls which receive the first power and which are respectively mounted on the first plurality of power ball mounts so as to electrically contact the first power line plane; and

a second plurality of power balls which receive the second power and which are respectively mounted on the second plurality of power ball mounts so as to electrically contact the second power line plane.

17. (new): The ball grid array package semiconductor device of claim 16, wherein the peripheries of the first and second power planes are each substantially rectangular.

18. (new): The ball grid array package semiconductor device of claim 16, wherein the first and second wiring are bonding wires.